APPENDIX **C**

Functional Description

This section provides a functional description of the system unit or server electronics.

C.1 System Unit / Server Overview

The processor-to-memory interconnection is provided by the UPA mechanism (FIGURE C-1). The output of the UltraSPARC processor(s) and the output of the system I/O (SYSIO) ASIC reside on the UPA. A slave UPA port is provided for graphic device communications between the UPA graphic(s), the BMX and CBT ASICs, and the SYSIO ASIC. All UPA interactions are controlled by the multi-processing system controller (SC-MP) ASIC.

The I/O sub-system connects to the processor-to-memory subsystem through the SYSIO ASIC. The SYSIO ASIC provides connectivity to four SBus slots, the fast Ethernet parallel port SCSI (FEPS) ASIC, the audio (APC) ASIC, and the Slavio ASIC.

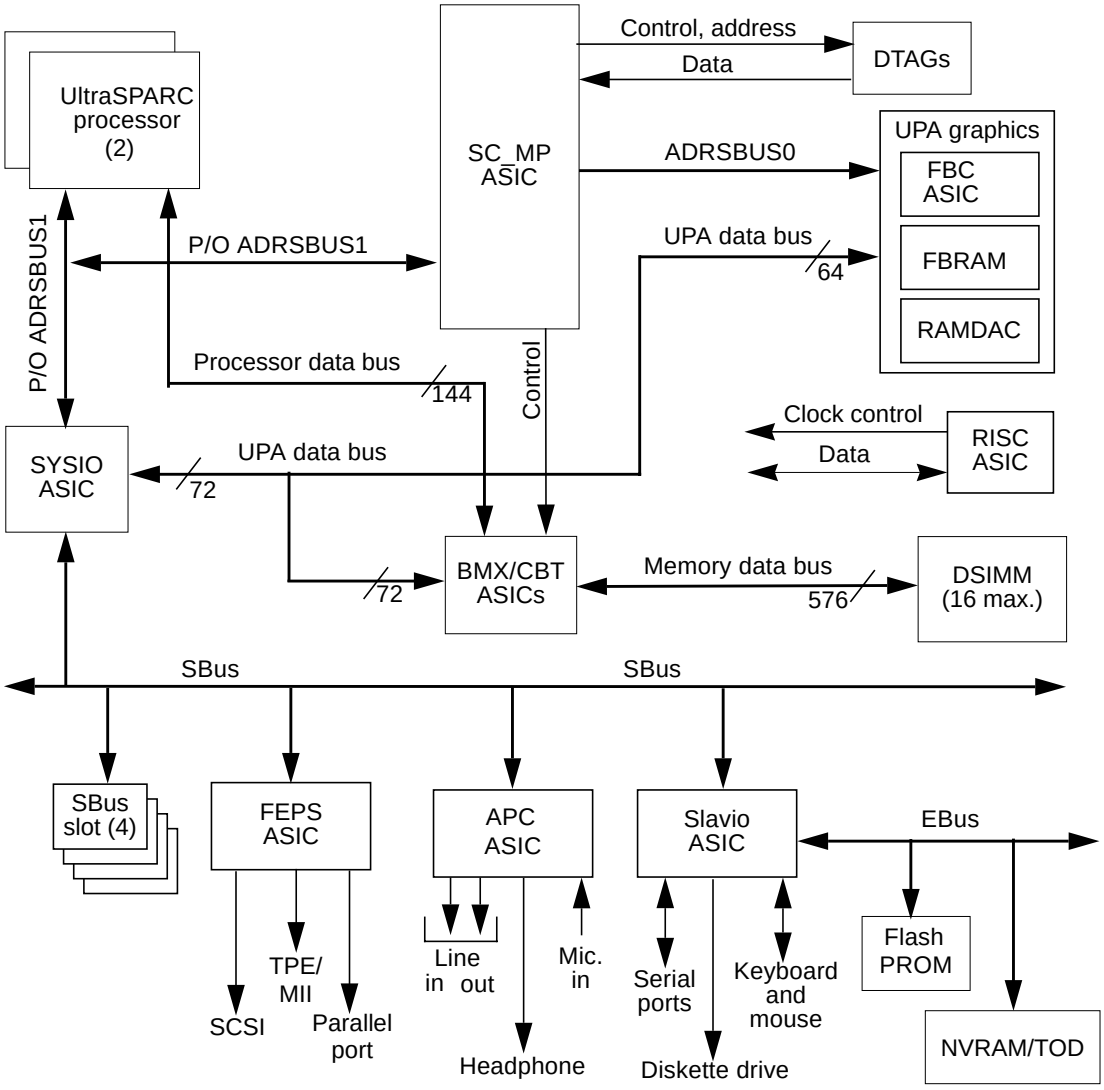

FIGURE C-1 System Unit or Server Functional Block Diagram

C.1.1 UPA

The UPA is a cache-coherent processor-to-memory interconnect. A key advantage of the UPA processor-to-memory interconnect is a scalable bandwidth through the support of multiple bussed interconnects for both data and address. Other advantages include more bandwidth, high-performance graphics support with two-cycle, single-word writes on the 64-bit UPA data bus, and centralized coherence and memory controller functions (see FIGURE C-1). The UPA consists of the following, as implemented on the motherboard:

- Eighteen buffered memory crossbar (BMX) ASICs and eighteen memory data multiplexer-demultiplexer (CBT) ASICs
  - The BMX ASICs connect the 144-bit UPA processor data bus to a 576-bit memory data bus through CBT ASICs, a 72-bit UPA data bus for graphics and I/O devices
  - The memory path is 576 bits using 18 CBT ASICs
- The processor(s) share(s) a UPA address bus (ADRSBUS1) with the SYSIO ASIC; a second address bus (ADRSBUS0) supports slave UPA connection to the expansion slot for graphics capability
- Low voltage transistor-transistor logic (TTL) voltage levels for signal input
- Low voltage complementary metal-oxide semiconductor (CMOS) voltage levels for signal output

UPA performance characteristics include:

- Peak bandwidth: 1.3-Gbytes per second with one 144-bit processor data bus on an 83-MHz UPA

C.1.2 SBus

The system unit or server uses the IEEE 1496 SBus specification. This includes (see FIGURE C-1):

- 16.6-MHz to 25-MHz operation. Default frequency is 25 MHz

Note – SBus frequency is independent of processor and UPA operating frequencies.

- Extended transfer mode (64-bit data path)
- Transfer sizes to 64 bytes (maximum)
- Parity
- Dedicated interrupts for each SBus slot.

The system unit or server supports four SBus slots. The four slots are configured in a side-by-side stacked configuration.

Note – The PrestoServe™ 2.4.2 release is incompatible with the Solaris 2.5.1 software environment when running on a Sun Ultra 2 Series system. For information about working around that problem, refer to *SMCC Open Issues Supplement Solaris 2.5.1*, part number 802-5340.

C.1.3 UltraSPARC I Processor

The UltraSPARC I processor is mounted on a module that is plugged into the system unit or server motherboard. Up to two modules are supported, one CPU for each module.

The UltraSPARC I processor has the following features (see FIGURE C-1):

- SPARC V9 compatibility:
  - V9 specifies a 64-bit instruction set architecture that is compatible with the 32-bit SPARC V8 architecture.
  - V9 provides for 64-bit data and addressing as well as other features to enhance operating system and application performance.
- Implements 44-bit virtual address bits and 41-bit physical address bits.
- Implements the visual instruction set (VIS) used by the UPA graphics device to provide optimal graphics performance (this also includes instructions to help with imaging performance).
- Execution of up to four instructions in parallel (one memory access, two integer ALU instructions, one floating point add class, one floating point multiply class, and one control transfer instruction).
- Each module receives a separate programmable core voltage to permit mixing of modules with different power requirements.
- Each module is thermo-coupled for temperature sensing; Ultra 2 series provides two levels; warning and shut-down.

UltraSPARC I processor performance characteristics include:

- 249 SpecInt92, 349 SpecFP92 for 168-MHz uniprocessor
- 332 SpecInt92, 505 SpecFP92 for 200-MHz multiprocessor

C.1.4 UltraSPARC II Processor

The UltraSPARC II processor is a high-performance, highly-integrated superscalar processor implementing the SPARC-V9 64-bit RISC architecture. The UltraSPARC II processor is capable of sustaining the execution of up to four instructions per cycle even in the presence of conditional branches and cache misses. This sustained performance is supported by a decoupled prefetch and dispatch unit with instruction buffer. The UltraSPARC II processor supports both 2-D and 3-D graphics, as well as image processing, video compression and decompression, and video effects through the sophisticated VIS. VIS provides high levels of multimedia performance, including real-time video compression / decompression and two streams of MPEG-2 decompression at full broadcast quality with no additional hardware support. The UltraSPARC II processor provides a 2-Mbyte ecache, with system operating frequencies from 250 MHz to 300 MHz.

UltraSPARC II processor characteristics and associated features include:

- SPARC-V9 architecture compliance
- Binary compatible with all SPARC application code
- Multimedia-capability VIS
  - Multiprocessing support
  - Glueless four-processor connection with minimum latency
- Snooping cache coherency
- Four-way superscalar design with nine execution units; four integer execution units
- Three floating-point execution units
- Two graphics execution units
- Selectable little- or big-endian byte ordering
- 64-bit address pointers
- 16-Kbyte non-blocking data cache
- 16-Kbyte instruction cache; single cycle branch following
- Power management
- Software prefetch instruction support
- Multiple outstanding requests

C.1.5 Memory

Memory uses conventional 5-Vdc DRAM SIMMs (DSIMMs) with a 60-ns access time (see FIGURE C-1).

The system unit or server memory configuration allows 4, 8, 12, or 16 DSIMMs with DSIMM memory capacity options of 16 Mbytes, 32 Mbytes, 64 Mbytes, or 128 Mbytes. Memory upgrades are in 4-DSIMM increments. Each DSIMM in a 4-DSIMM group must contain the same memory capacity if not, the lower of the DSIMM memory capacities determines the other DSIMM capacities.

Characteristic memory performance includes a peak memory read bandwidth of 667 Mbytes per second and a peak memory write bandwidth of 485 Mbytes per second with random accesses to the DRAM using eight or more DSIMMs. FIGURE C-2 shows the DSIMM group and bank layout.

Note –

Two pairs of DIMMs form a group of four DIMMs.

All four DIMMs within a group must be the same size.

The minimum memory requirement is four DIMMs in Group 0.

DIMMs can be installed in Group 1, Group 2, or Group 3 in any order.

Each group addresses 512 Mbytes of memory. Unused memory is mapped out by the memory management hardware.

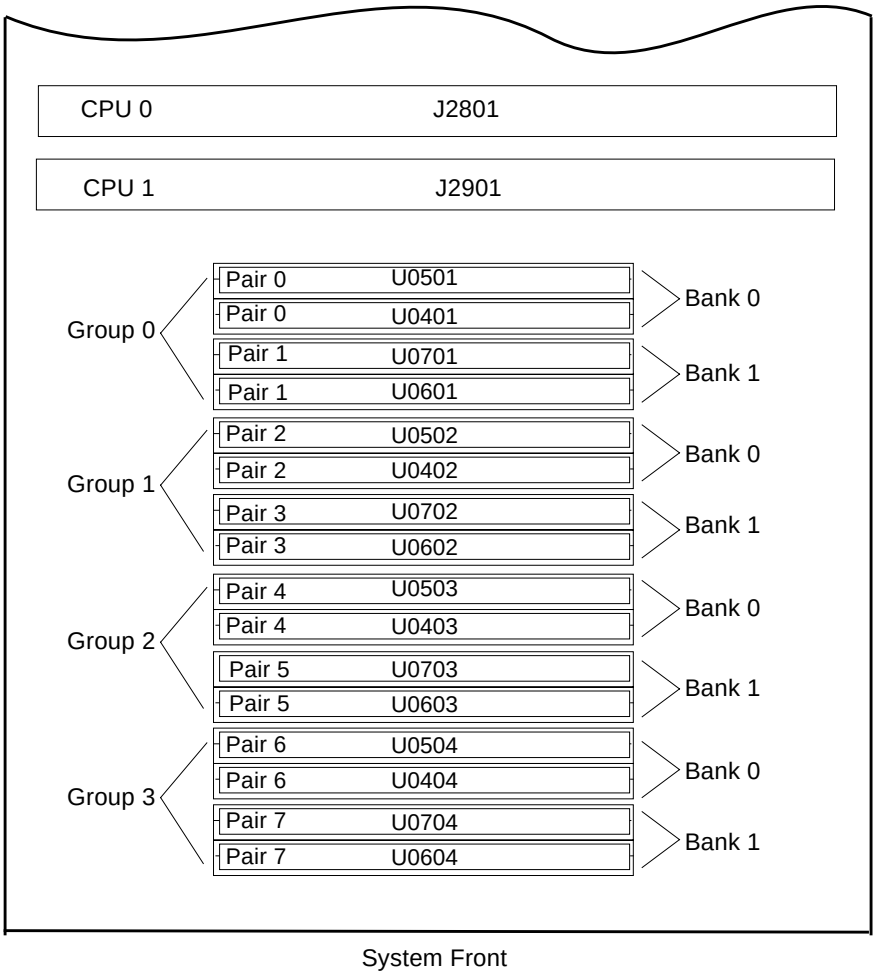

FIGURE C-2 DSIMM Group and Bank Layout

C.1.6 Graphics and Imaging (Workstation Only)

The system unit takes advantage of UPA features to provide high performance UPA graphics. An FBC ASIC provides acceleration for 2-D and 3-D imaging primitives (see FIGURE C-1).

The UPA graphics consist of the FBC ASIC, the FBRAM, RAMDAC, and associated circuitry. The UPA graphics connect to the system unit through the UPA64S expansion connector.

FBRAM is a standard DRAM that includes a multilevel cache. The FBC ASIC permits a write-mostly interface. This feature, combined with the 3DRAM cache and support for graphics operations, provides for a high performance frame buffer.

UPA graphics support the VESA standard for monitor control. UPA graphics also support stereo video.

Configuration restrictions:

- UPA graphics configuration are configured to operate the FBRAM interface at 66-MHz; single-buffer (SB), double-buffer plus Z (DBZ); or 75-MHz for the DBZ speed-sort.
- ZX is supported as an optional upgrade only.

C.1.6.1 Graphics Card Features

Features provided by the UPA graphics card include:

- YCC-to-RGB color space conversion for faster video decompression
- Contrast stretch support for imaging
- Line doubling for interlaced video writes
- Consecutive block prefetch for smart frame buffer reads
- DDC2B monitor serial communication with EDID default resolution support in the boot PROM
- 3DRAM OpenGL stencil function (four planes) support
- New RAMDAC support
- Single-buffered high-resolution (2.5 Mpixels) supports the following screen resolutions (DBZ graphics card only):
  - 1920 × 1360 pixel landscape mode (HDTV)
  - 1280 × 2048 pixel portrait mode (medical)
- Buffer B addressing for stateless (dumb frame buffer) and video accesses
- Simultaneous 8-bit and 24-bit visual support
- Multiple hardware color maps

- Programmable gamma correction; four-color lookup tables help eliminate color flashing within an 8-bit window system environment
- Texture cache for texture mapping
- Acceleration for X11 and XIL graphics libraries
- Acceleration for 3-D applications (XGL, OpenGL, and Java3D)
- 3-D solids, dynamic shading, rotation, and Z-buffered acceleration
- High resolution (1280 x 1024 pixels at 76 Hz, non-interlaced)
- Stereo ready (960 x 680 pixels at 122 Hz, non-interlaced)
- Dedicated graphics floating-point processing (can turn on more light points for enhanced visual display without a performance penalty)

C.1.6.2 Graphics Card Performance

The UPA graphics cards have identical window system performance characteristics, 2-D graphics, and imaging and video applications. In addition, the UPA graphics cards provide very fast, high-quality transformation and display of 3-D solid and wireframe objects and dramatically accelerate high-end functionality like double buffering, triangle and quad rendering, and lighting and shading. At the same time, the UPA graphics cards accelerate 2-D objects that meet X11 rules. Fast 8- and 24-bit window system and imaging performance are provided along with acceleration for decompression and display of compressed digital video.

C.1.6.3 Graphics Not Supported

The following graphics are not supported in the Ultra 2 series systems:

- GS SBus graphics accelerator (370-1329, 370-1370, 370-1407, and 370-1551)
- GT graphics subsystem (501-1624, 501-1692, 501-1694, and 501-1726)
- GT2 graphics subsystem SBus adapter card (501-1693)
- GX (501-1481 and 501-1645)
- GX+ (501-1717, 501-2018, and 501-2039)
- ZX2 (501-1694)

C.1.7 Peripherals

The following peripherals are supported by the system unit or server:

- CD-ROM drive
- Diskette drive
- Hard drive

A small computer system interface (SCSI) and optional tape drive components; 4-mm and 8-mm are also supported.

C.1.7.1 CD-ROM Drive

The CD-ROM drive is a standard device with multimedia features. This includes multisession capability and fast access for image and video data. Headphone access, eject, pin eject, and volume control is available on the front panel. Audio from the CD is available through either the front panel headphone connection, the line-out connector at the system unit or server rear (accessible by cabling from front to rear), or the internal speaker. The *SunCD 4 Drive Specifications*, document part number 802-4157, provides cleaning, jumper setting, and operating instructions for the 4x CD-ROM drive and the *SunCD 12X Installation and User's Guide*, document part number 805-0940, provides cleaning, jumper setting, and operating instructions for the 12x CD-ROM drive (see FIGURE C-1).

Note – Both multifunction and quadra-speed CD-ROM drives are supported as long as they conform to the 5.94-inch x 7.78-inch x 1.71-inch (15.10-cm x 19.80-cm x 4.30-cm) dimensions.

C.1.7.2 Diskette Drive

The system unit or server uses a standard 1.44-Mbyte diskette (floppy) drive that is 1 inch (2.50 cm) high. The system unit- or server-to-diskette drive interface is a 82077 style interface (see FIGURE C-1).

C.1.7.3 Hard Drive

The system unit or server supports two 1-inch drive bays that may hold a total hard drive storage capacity of 18.2 Gbytes. Each drive has a 3.5-inch (8.90-cm) form factor with a single connector configuration. A drive bracket is used to mount the drive to the system unit or server (see FIGURE C-1). TABLE C-1 lists the supported hard drives.

TABLE C-1 Supported Hard Drives

Form Factor Dimension	Hard Drive Capacity	Fast/Wide SCSI	RPM	Access Time
1 inch	535 Mbytes	No	4500	12 ms
1 inch	1 Gbyte	Yes	5400	11 ms
1 inch	2.1 Gbytes	Yes	7200	9.5 ms
1 inch	4.2 Gbytes	Yes	7200	9.5 ms
1 inch	9.1 Gbytes	Yes	7200	9.5 ms

C.1.8 SCSI

The system unit or server provides a 20-Mbyte per second SCSI interface that is supported by the FEPS ASIC. 20 Mbytes per second is provided by 16-bit single-ended operation at 10 MHz. Both internal and external peripherals are connected to the same daisy chain. External connection is provided through a 68-pin SCSI connector (see FIGURE C-1).

System configuration requires external devices to be connected in a daisy chain configuration. A maximum of 12 external devices may be daisy-chained through a maximum cable length of 19.69 feet (6 meters). The end of the daisy chain must be terminated with an active terminator. If both 50-pin and 68-pin external devices are connected externally, the 68-pin device must be connected earlier in the daisy chain. A special terminator is available for the last 68-pin device that terminates the extra signals and converts the extra signals into a 50-pin configuration. The last 50-pin device must be terminated.

Note – When using the 535-Mbyte hard drive, contact your Sun representative to order a 50-to-68-pin SCSI cable: for 1.2-meter (1.3-yard) external SCSI cable, order X903A; for 2.0-meter (2.2-yard) external SCSI cable, order X904A.

C.1.8.1 SCSI Implementation

- Single-ended
- 16-bit (wide SCSI) with parity
- 20 megabits-per-second (Mbps) Fast/Wide SCSI
- Supports 16 SCSI addresses:
  - Targets 0 - 6 and targets 8 - F for devices
  - Target 7 reserved for motherboard SCSI host adapter
- Supports up to three internal SCSI drives:
  - SCSI hard drive target 0 (lower drive slot)
  - SCSI hard drive target 1 (upper drive slot)
  - SCSI CD-ROM drive target 6 or SCSI tape drive target 5
- External 8-bit and 16-bit SCSI devices supported through a 68-pin SCSI connector

C.1.8.2 SCSI Cabling and Configuration

When mixing 8-bit and 16-bit SCSI devices on the same physical SCSI bus, follow these cabling and configuration guidelines to insure proper device addressing and operation:

- If all external mass storage devices use 68-pin connectors, connect all non-Sun devices to the Ultra 2 Series system first, followed with Sun devices. Sun devices use autotermination.
- If external mass storage devices consist of 68-pin Sun devices and 50-pin devices, connect the Sun 68-pin devices to the Ultra 2 Series system first and terminate the daisy chain with the 50-pin device and its terminator.

Figure 1-8 provides an illustrated summary of cabling and configuration guidelines.

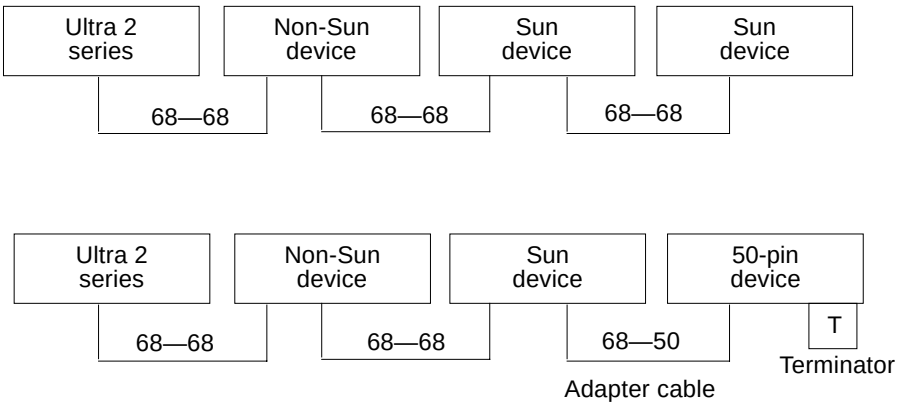

FIGURE C-3 Connecting External Mass Storage Devices

C.1.9 Optional 4-mm and 8-mm Tape Drives

The system unit or server supports the optional 4-mm and 8-mm tape drives. Either the 4-mm tape drive or the 8-mm tape drive may be installed in the system or server unit in place of the CD_ROM drive.

C.1.9.1 4-mm Tape Drive

The 4-mm tape drive is equipped with a single-ended SCSI controller and a 1-MByte on-drive buffer. The *4-mm Tape Drive Specifications*, document part number 802-5324, provides cleaning, jumper setting, and tape cartridge instructions for the 4-mm tape drive.

C.1.9.2 8-mm Tape Drive

The 8-mm tape drive is an enhanced 8-mm digital helical-scan cartridge tape subsystem. It is packaged in the industry standard 5.25-inch (13.335-cm) half-height form factor. The *8-mm Tape Drive Specifications*, document part number 802-5775, provides cleaning, jumper setting, and tape cartridge instructions for the 8-mm tape drive.

C.1.10 Networking

The system unit or server supports 10-Mbit and 100-Mbit local area Ethernet IEEE standard 802.3u (also known as 100BASE-T) through the FEPS ASIC. The FastEthernet standard is backwards-compatible with the standard 10-Mbits per second Ethernet standard. The speed is auto-sensed.

Twisted-pair Ethernet (TPE) support is provided through a RJ45 connector. In addition, a media independent interface (MII) connection provides support to any other form of Ethernet (AUI/TP/ThinNet). The MII connection is provided through a 40-pin MII connector. MII converters include MII-to-AUI and MII-to-fiber optic.

Note – The MII-to-AUI converter connects the MII connector on the backpanel of the Sun Ultra 2 series system unit or the SunFastEthernet™ adapter to AUI 10BASE-5 DB-15 Ethernet connectors. Contact your Sun representative to order an MII-to-AUI converter, order X467A.

C.1.11 10BASE-T TPE Link Test

This section contains important information for getting your system to communicate correctly over a 10BASE-T TPE network. If you have no experience with TPE networks, ask your system or network administrator to perform the procedures in this section.

Note – This section *does not* apply to 100BASE-T networks. In such networks, the link test function must be enabled at both the host and the hub. If your host is connected to a 100BASE-T network, you must not disable the host link test function.

C.1.11.1 Overview

- The TPE link integrity test is a function defined by the IEEE 802.3 10BASE-T specification.
- For a networked workstation (host) to communicate with a network hub, the link test state (enabled or disabled) must be the same on the host and hub.
- If either the host or hub does not share the link test enabled / disabled state of the other, then the host cannot communicate effectively with the hub, and the hub cannot communicate effectively with the host.

FIGURE C-4 illustrates an example of a star configuration local area network (LAN), showing the host(s)-to-hub relationship. FIGURE C-5 shows the importance of ensuring that the host-to-hub link test settings match in a 10BASE-T network.

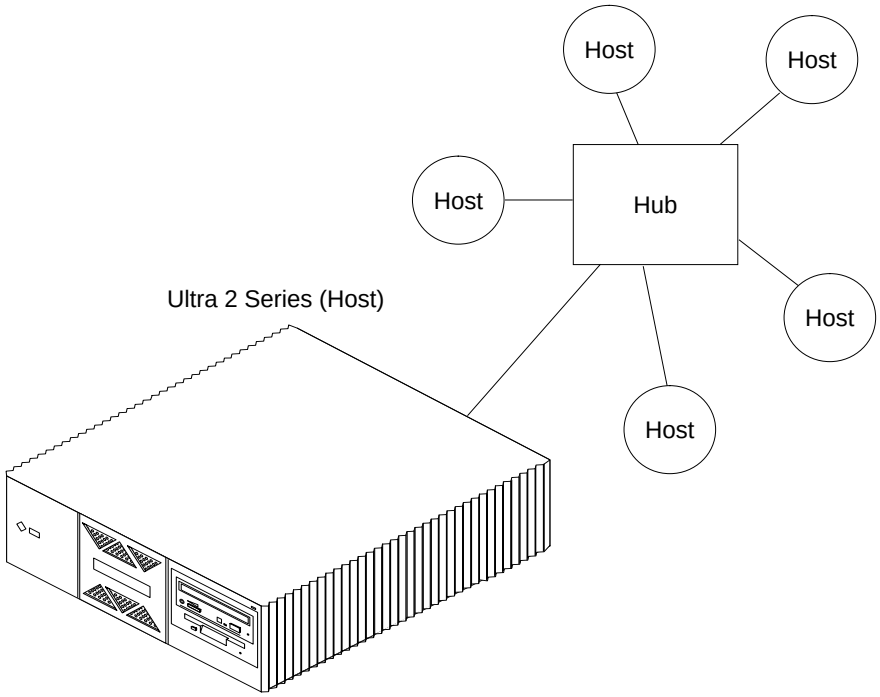

FIGURE C-4 Host(s)-to-Hub Star Configuration LAN

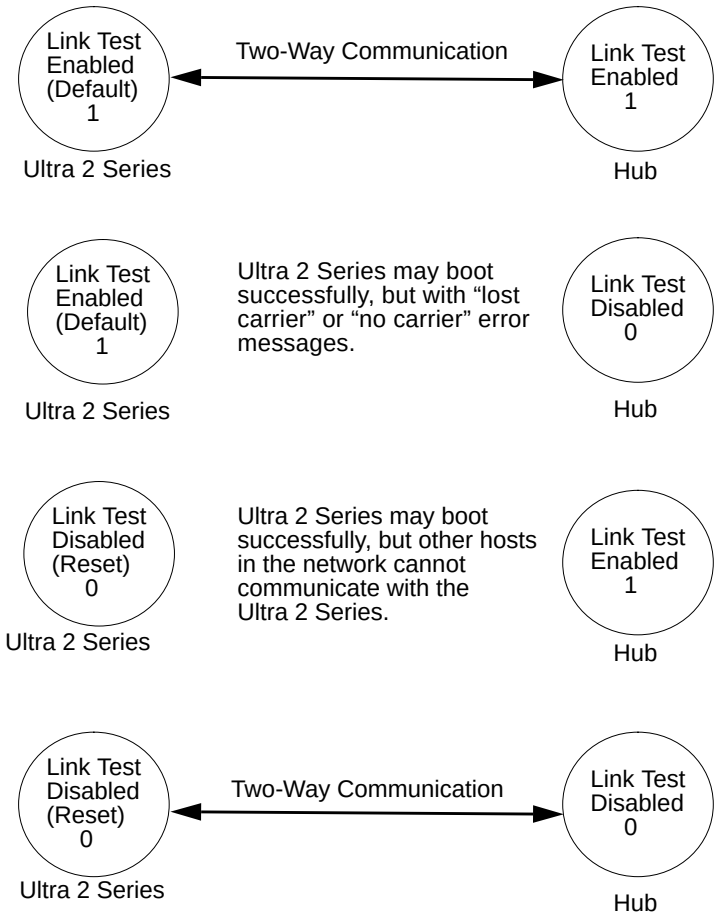

FIGURE C-5 Ensuring a 10BASE-T Host-to-Hub Communication Network

C.1.11.2 Technical Discussion

The TPE link integrity test determines the state of the twisted-pair cable link between the network host and hub. Both the host and hub regularly transmit a link test pulse. When either the host or hub has not received a link test pulse within a certain amount of time (50 - 150 ms), it makes the transition from the link-pass state to the link-fail state and remains in the link-fail state until it once again receives regular link test pulses.

The link integrity test is specific to TPE and is not applicable to the other physical layer implementations of IEEE 802.3 such as 10BASE5 (thicknet) or 10BASE2 (thinnet).

The link test function at the host or hub is either enabled (link test enabled or 1) or disabled (link test disabled or 0). The IEEE 802.3 10BASE-T specification requires that the link test be enabled at both the host and the hub.

Although link test disabled does not conform to the specification, it is often encountered in real-world 10BASE-T network installations. Some hubs from various vendors can exhibit any of the following:

- Link test is “hardwired” enabled — link test is always enabled.
- Link test is “hardwired” disabled — link test is always disabled.
- Link test is configurable — the network administrator may enable or disable link test.

C.1.11.3 Troubleshooting

If you have connected an Ultra 2 Series host to a hub using TPE cable and observe either “no carrier” messages or fail to communicate effectively with another host in the same network, look first at the hub. If it supports configurable link test, then make sure “link test enabled” is configured. This is usually done by setting a hardware switch.

If the hub does not support configurable link test, then refer to the hub manufacturer’s documentation. Check to see if your hub is hardwired for link test disabled. If it is, refer to Section C.1.11.5 “Checking or Disabling the Link Test” on page C-19 to disable the link test at your Ultra 2 Series host.

C.1.11.4 Moves and Changes

If the Ultra 2 Series host is physically moved to another network location or if the hub is reconfigured, remember to refer back to FIGURE C-5. Unless the new network relationship between the host and the hub is functional (that is, 1-1 link test enabled-link test enabled or 0-0 link test disabled-link test disabled), there will be no full, regular two-way communication between the host and the hub.

C.1.11.5 Checking or Disabling the Link Test

To check the link test:

1. **If you do not see the** `ok` **prompt, press the Stop (L1) and A keys.**
2. **At the** `ok` **prompt, type:**

```
ok printenv tpe-link-test?
tpe-link-test?        true                true
ok
```

Note – The above screen shows the current link test state (true, or enabled), followed by the default state (true, or enabled).

To disable the host's link test:

1. **Type the following commands:**

```
ok setenv tpe-link-test? false
tpe-link-test? =    false
ok reset-all
```

2. **Boot the host. Verify that the transceiver cable problem messages do not appear. Type either** `boot net` **or** `boot disk` **and press Return.**

C.1.11.6 Enabling the Link Test

1. **If you do not see the** `ok` **prompt, press the Stop (L1) and "A" keys.**
2. **At the** `ok` **prompt, type**:

```
ok printenv tpe-link-test?
tpe-link-test?        false               true
ok
```

Note – The above screen shows the current link test state (false, or disabled), followed by the default state (true, or enabled).

---

3. **To enable the host's link test function, type the following commands**:

```
ok setenv tpe-link-test? true
tpe-link-test? =    true
ok reset-all
```

4. **Boot the host and verify that the transceiver cable problem messages do not appear. Type either** `boot net` **or** `boot disk` **and press Return.**

C.1.12 Terminal, Modem, Keyboard, and Mouse Connectivity

Terminal, modem, keyboard, and mouse connectivity is traditional Sunness connectivity (see FIGURE C-1). Two serial ports provide synchronous and asynchronous communication. The synchronous port supports data throughput rates up to 64 Kbaud. The asynchronous port supports data throughput rates up to 76.8 Kbaud.

Both RS-232 and RS-423 interface standards are supported. RS-232 or RS-423 interface selection is provided through a jumper setting. Default configuration is RS-423. Two DB25 connectors are provided for the two serial ports.

Keyboard and mouse functionality is provided through a DIN8 connector. Sun Type-5 keyboards and a new mechanical mouse are supported.

C.1.12.1 Setting Up the Modem

Any modem compatible with U.S. Robotics or CCITT V.24 can be connected to the Ultra 2 Series serial ports. Modems can be set up to function in one of three ways:

- Dial out only
- Dial in only
- Bidirectional calls

To set up your modem:

1. **Become superuser and type** `admintool`**.**

```
% su
Password:
# admintool
```

2. **Highlight** `Browse`**.**
3. **Select** `Serial Port`**.**
4. **Select Port A or Port B for your modem connection.**
5. **Select** `Edit`**.**
6. **Select** `Expert`**.**
7. **Open the** `Use Template` **menu, and select one of the following**:
   - `Modem - Dial-Out Only`
   - `Modem - Dial-In Only`
   - `Modem - Bidirectional`
8. **Select** `Apply`**.**
9. **Set your modem auto-answer switch to one of the following**:
   - For `Dial-Out only`, set the switch to Off.
   - For `Dial-In Only`, set the switch to On.
   - For `Bidirectional`, set the switch to On.

C.1.12.2 Serial Port Speed Change

You must edit the `/etc/remote` file to change the speed of a serial port:

1. **Become rootsuperuser, and type** `cd /etc`**.**

```
% su
Password:
# cd /etc
```

2. **Type** `vi remote`**.**
3. **Type** `tip speed device-name`**.**
4. **Typical speeds are 9600, 19200 to 38400 bps. The device name is the serial port name — for example,** `/dev/tty[a,b]` **or** `/dev/term/[a,b]`**.**
5. **Press Esc and type** : `wq` **to save your file change(s) and to exit from the** `vi` **text editor.**

C.1.12.3 Recommendations

Cable

For a modem-to-host (system) connection, use an RS-423/RS-232 straight-through cable with DB-25 male connectors at both ends.

Modem Switch Settings (AT Commands)

- Enable transmit flow control (AT&H1) [suggested setting] (required for sending binary/8-bit data)
- Set link rate to fixed (will not track modem data rate, AT&Bn; n equals menu choice in modem manual.)
- Set display result codes (ATQ0)
- Set verbal result codes (ATV1)
- Set result code subset (ATXn; n equals option choice)
- Save settings in NVRAM (AT&W)

Note – The above settings are guidelines to help you get started quickly. Changes to these guidelines should be expected depending on your site requirements and the modem you are using. For additional information about modem switch settings, see the manual that came with your modem.

C.1.13 Printer Connectivity

Parallel printer port connectivity is provided with a DB25 connector. This interface supports up to two Mbytes-per-second data throughput and is Centronics-compatible. All SPARC printers are supported (see FIGURE C-1).

C.1.14 Audio

Audio includes interface, built-in speaker, and microphone (see FIGURE C-1).

C.1.14.1 Interface

The system unit or server includes the Codec for audio functionality. Four external connectors are supplied: line input, line output, a headphone, and stereo microphone. All connectors are 0.125-inch (3.5-mm) mini-stereo connectors. Line-in and line-out connectors support 16-bit CD quality stereo. TABLE C-2 lists each audio port function. TABLE C-3 identifies the audio input and output specifications.

TABLE C-2 Audio Port Functions

Port	Function
Headphones	Connects stereophonic headphones for private listening of audio output
Line Out	Connects the system audio output to an external stereophonic amplifier and loudspeakers
Line In	Connects external stereophonic audio sources such as a compact disc player or cassette tape player to the system
Microphone	Connects the SunMicrophone II (or other suitable microphone[1]) to the system

1. The Ultra 2 series microphone port accepts stereophonic input; however, the Sun Microphone II is a monophonic device. Note also that the older SunMicrophone is not compatible with the Ultra 2 Series system.

TABLE C-3 Audio Inputs and Outputs[1]

Stereo I/Os	Specifications
Line In	2V typical, 4V max.; 5-50–ohm impedance
Frequency Response	20 Hz to 17 kHz (+/- 0.5 dB)
Internal CD Input	
Input Level	0.1 Vrms typical at 10 kohms; 2Vpp max.
Distortion	0.01percent, typical at 1 kHz
S/N Ratio	84 dB, typical IEC 179 A-weighted
Frequency response	20 Hz to 17 kHz (+/- 0.5 dB)
Microphone Input[2]	15 mV typical, 0.6 to 1.0 kohm impedance;
	+5 VDC input bias through a 2.2-kohm resistor
Headphone Output	1V typical, 2.4V max.; 16-ohm to 1-kohm impedance
Line Out	1V typical, 2.4V max.; 5-ohm to 50-kohm impedance

1. Specifications listed in Table C-3 assume that the audio tool format setting, “CD-ROM or DAT” is selected.
2. The microphone input specifications are for the SunMicrophone II.

C.1.14.2 Built-in Speaker

The system unit or server contains a cost-effective speaker. The speaker provides audio functionality in the absence of external speakers. Audio from all sources is available. TABLE C-4 lists the built-in speaker specifications.

TABLE C-4 Built-in Speaker Specifications

Speaker	Specifications
Power output	1.5 W average, 3 W peak
Distortion	0.02 percent, typical at 1 kHz
Impedance	16 ohms (+/- 20 percent)
Frequency response	150 Hz to 17 kHz (+/- 0.5 dB)

C.1.14.3 Microphone

A SunMicrophone II mono microphone is included with each system unit.

C.1.15 ASICs

The system unit or server achieves a high level of integration through application-specific intergrated circuits (ASICs). All ASICs are 1149.1 (JTAG) compliant. The following ASICs are highlighted and are described in the following subsections:

- SC_MP—page C-26
- SYSIO—page C-26
- BMX—page C-27
- RISC—page C-27
- FEPS—page C-28
- SLAVIO—page C-29
- CBT—page C-29

TABLE C-5 lists each ASIC by name and provides characteristics of each device.

TABLE C-5 ASIC Characteristics

ASIC Name	Gates	RAM (bits)	Package	Die Size (mm x mm)	Power (W)	Reqd Per Unit
SC_MP	140K	0	372BGA		3.9	1
SYSIO	116K	14K	372BGA	10 x 10	2.7	1
BMX	7K	0	44TSSOP	NA	0.2	18
RISC	7k	0	160MQFP	6.25 x 6.25	0.4	1
FBC	202K	16K RAM, 32K ROM	313BGA	10.54 x 10.54	5.9	1
CBT	0.4K	0	56TSSOP	NA	0.2	18
RAMDAC			208PQFP	NA	2.0	1
FEPS	115K	4K	240PQFP		2.0	1

C.1.15.1 SC_MP

The multiprocessing system controller (SC_MP) ASIC is the key element for controlling the UPA and main memory. The SC_MP ASIC controls accesses from UPA master device to UPA slave device, and UPA accesses to memory. SC_MP includes a complete coherency controller which controls system dual tags (DTAGs).

The SC_MP ASIC:

- Integrates memory controller functionality. Memory controller is programmable to accommodate multiple DRAM and UPA speeds
- Supports four groups of memory, each with four DSIMMs
- Supports 16-Mbyte, 32-Mbyte, 64-Mbyte, and 128-Mbyte, 60-ns DSIMMs
- Supports maximum memory configurations of 2 Gbytes with sixteen 128-Mbyte DSIMMs
- Supports three UPA masters and one UPA slave with independent address busses (independent busses are required for graphics streaming)
- Controls the BMX ASIC which connects the UPA data bus and memory
- Controls the CBT ASICs

C.1.15.2 SYSIO

The system I/O controller (SYSIO) ASIC bridges between the UPA and the SBus.

The SYSIO ASIC:

- Contains the IOMMU
- Integrates streaming buffer to enhance sequential I/O performance
- Provides logic for dispatching interrupt vectors to processors
- Provides ECC generation and checking logic

C.1.15.3 BMX

The buffered memory crossbar (BMX) ASIC is a three-port crossbar connecting one 144-bit UPA data bus, one 288-bit-wide DRAM memory bus, and one 72-bit UPA data bus. To maintain a manageable pin count, the devices are sliced so that 18 BMX ASICs are needed to form the complete switch function.

The BMX ASIC includes:

- 8 bits of UPA 128, 4 bits of UPA 72, and 16 bits of DRAM bus per ASIC
- Switch connections controlled by SC

C.1.15.4 RISC

This reset, interrupt, scan, and clock (RISC) ASIC implements four functions: reset, interrupt, scan, and clock. Generation and stretching of the reset pulse is performed in this ASIC. Interrupt logic concentrates 42 different interrupt sources into a 6-bit code which communicates with the SYSIO ASIC. The RISC ASIC also integrates a JTAG controller. In cases where there are multiple processors, they are required to run at the same frequency. A 3-bit code is output by each processor module to indicate the speed for that module. Logic inside the RISC ASIC determines the minimum value of the processor codes, and outputs the selected value for the remaining clock logic to set the main system frequency.

The RISC ASIC:

- Determines system clock frequency
- Controls reset generation
- Provides JTAG
- Performs SBus and miscellaneous interrupt concentration for SYSIO
- Controls flash PROM programming, frequency margining, and lab console operation
- 25-MHz operation

C.1.15.5 FEPS

The fast Ethernet parallel port (FEPS) ASIC provides throughput for I/O devices connected to the Ethernet, SCSI, and parallel port interfaces. The FEPS ASIC consists of a frame buffer controller ASIC and a RAMDAC ASIC.

The FEPS ASIC:

- Integrates 20-Mbyte per second SCSI interface core with low system overhead
- Integrates 10-Mbit per second and 100-Mbit per second Ethernet
- Complies with IEEE 1496 SBus specification. Also provides for 64-bit SBus transfers
- Supports SBus extended transfer and 64-byte burst transfer
- Provides 25-MHz SBus operation

FBC

The frame buffer controller (FBC) ASIC is the graphics draw ASIC that interfaces to the UPA and to the UPA graphics FBRAM. The FBC ASIC provides graphics draw acceleration.

The FBC ASIC:

- Includes a UPA slave device with write-mostly philosophy
- Supports single-buffered and double-buffered with Z buffer configurations
- Interfaces with 3DRAM to achieve accelerated graphics performance
- Supports frame buffer to frame buffer copy
- Supports viewport clipping, picking, and pixel processing
- Supports byte, plane masks, raster operations, blend operations, and conditional writes in 3DRAM

RAMDAC

The RAM digital-to-analog converter (RAMDAC) ASIC is listed for reference. It is being designed in conjunction with an outside vendor.

The RAMDAC ASIC includes:

- Built-in VTG
- Direct interface to FBRAMs
- On-board phase-lock loop (PLL) and clock generator circuitry for the pixel clock
- 64 X 64 cursor LUT
- Direct support for X visual types

C.1.15.6 SLAVIO

The slave I/O (SLAVIO) ASIC provides most of the Sunness I/O requirements. It contains serial ports, floppy control, and extended bus (EBus) control.

The SLAVIO ASIC includes:

- Highly integrated for supplying Sunness I/O requirements
- Integrated keyboard/mouse interface
- Compliance with IEEE 1496 SBus specification
- 25-MHz SBus operation

C.1.15.7 CBT

The memory data multiplexer and de-multiplexer (CBT) ASIC is a two-port switch between a 576-bit memory bus (DSIMM side) and 288-bit memory bus (BMX side). To maintain a manageable pin count, the CBT ASICs are sliced into 18 parts to form the complete switch function.

The CBT ASIC provides:

- 16 bits of MEMORY 288 bus and 32 bits of DRAM bus per ASIC
- 5-VDC power supply voltage
- Switch connections controlled by SC_MP ASIC

C.2 Power Supply

TABLE C-6 lists power budgets for the Ultra 2 series desktop workstation and the Ultra Enterprise 2 server power supply.

The power supply provides:

- Remote sensing on +3.0 VDC, +3.3 VDC, and +5.0 VDC
- Six cables that are required for power distribution: one to the CD-ROM drive, one to the diskette drive, and four to the motherboard

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Note – Motherboard cables consist of two for the programmable voltages, one for other voltages, and one for sensing.

- A programmable supply that ranges from 2.5 VDC to 3.5 VDC. The programmable voltages are controlled by the CPU module(s) to permit CPU modules having different core voltages to operate conjointly within the same system unit or server.

Note – Power values listed in TABLE C-6 translate to worse-case current requirements. Peak current requirements are greater. Note that the amount of power dissipated as heat is not listed. Also, the maximum delivered power is not the same as the sum of the output powers because of configuration restrictions and peripheral power-dissipation limits that are smaller than peak current requirements. All component power supply budget values are measured as a function of wattage.

TABLE C-6 Ultra 2 Series Workstation / Server Power Supply Budget

Component	3.3Vdc	Programmable (2x)	5Vdc	+12Vdc	-12Vdc	Maximum Power Delivered
UltraSPARC module (2x)[1]	30.0	70.0	0.0	0.0	0.0	100.0
Memory	0.0	0.0	45.0	0.0	0.0	45.0
Graphics (double-buffer, desktop workstation only)	16.0	0.0	2.5	0.5	0.0	19.0
Motherboard	12.3	0.0	6.6	17.7	0.5	37.1
SBus (4 slots)	0.0	0.0	40.0	4.8	4.8	40.0
Disks (2x)	0.0	0.0	<15.0	<28.8	0.0	30.0
CD-ROM drive	0.0	0.0	<6.0	<12.0	0.0	12.0
4-mm tape drive	0.0	10.0	5.5	6.0	0.0	10.0
8-mm tape drive	0.0	0.0	12.0	8.4	0.0	15.0
Diskette drive	0.0	0.0	1.5	0.0	0.0	1.5
Keyboard / mouse (desktop workstation only)	0.0	0.0	1.6	0.0	0.0	1.6
Output sized to	**182.0**	**80.0**	**125.0**	**76.5**	**4.1**	
Total						**311.2**

1. Power supply budget measurements for two 168-MHz UltraSPARC modules. Power supply budget values for two 200-MHz UltraSPARC modules are somewhat less.

C.3 Power Management

To meet EPA Energy Star requirements, the system unit power consumption is lower than 30 watts.

In system unit software monitors system unit activity and based on the system unit control settings, system unit software saves the machine state (including the memory) onto the hard drive and halts the operation system. The system unit software then turns off the power supply.

Based on the setting of the NVRAM/TOD, which has an alarm clock, the system unit is turned on automatically if the alarm is set. This is done by having the interrupt out of the NVRAM/TOD directly connected to the power supply. The power supply requires a power_off signal for the system unit software to be able to write to a bit within a register and have the power supply shut down.

Note – If you experience RED State Exception failures when exercising Energy Star suspend/resume functions, install patch 104729-01. An alternative is to install the Solaris 2.5.1 Hardware: 4/97 release, which also incorporates a correction to this problem.

C.4 Motherboard

FIGURE C-6 illustrates a block diagram of the Ultra 2 series motherboard.

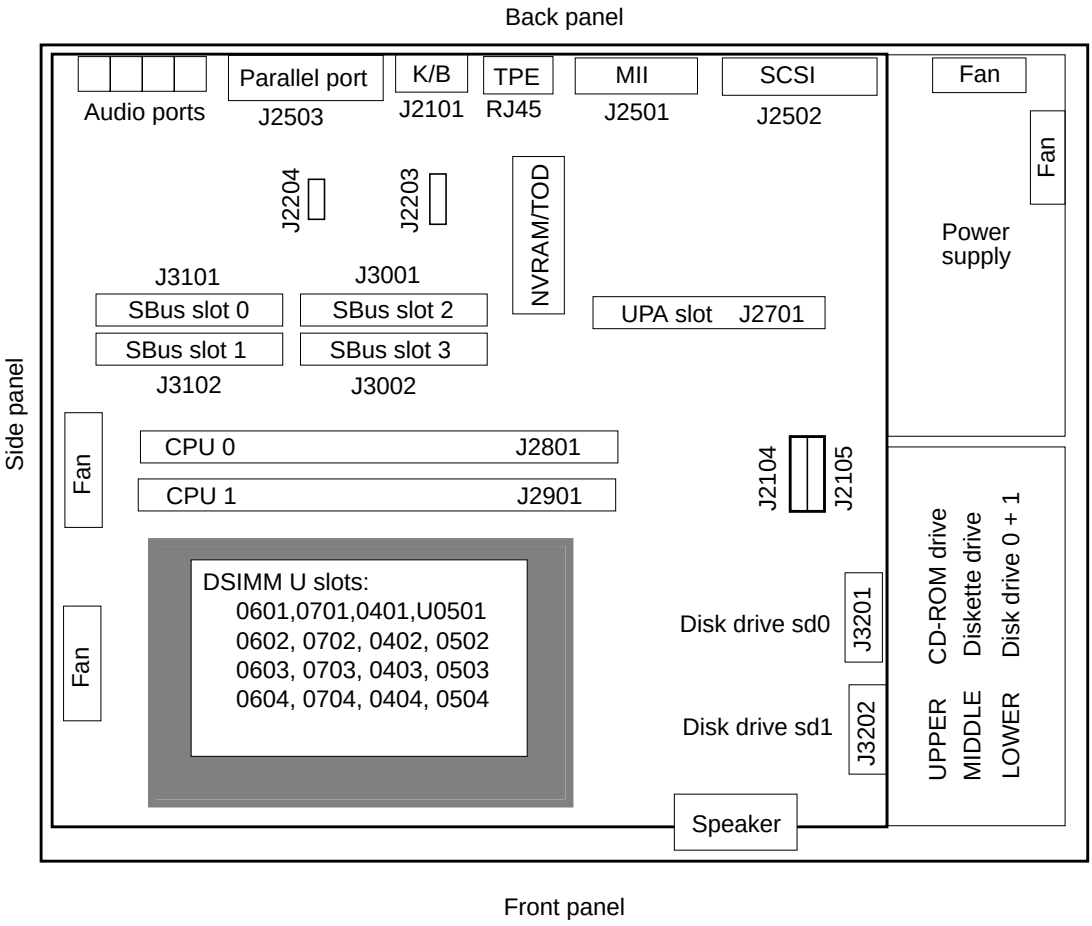

FIGURE C-6 Ultra 2 Series Motherboard Block Diagram

C.5 Jumper Description

Jumper configurations can be changed by setting jumper switches on the motherboard. The motherboard's jumpers are preset at the factory.

A jumper switch is *closed* (sometimes referred to as shorted) with the plastic cap inserted over two pins of the jumper. A jumper is *open* with the plastic cap inserted over one or no pin(s) of the jumper. FIGURE C-7 shows the different jumper settings that are used on the motherboard.

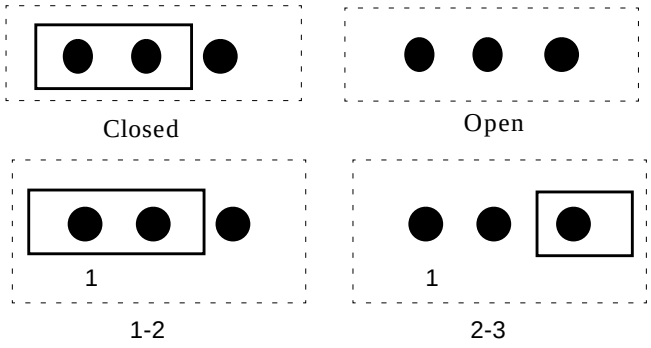

FIGURE C-7 Selected Jumper Settings

The jumper description includes a brief overview of serial port jumpers, flash PROM jumpers, and additional motherboard jumpers and connector blocks.

Jumpers are identified on the motherboard by J designations. FIGURE C-8 distinguishes jumpers with identifying asterisks. Jumper pins are located immediately adjacent to the J designator. Pin 1 is marked with an asterisk in any of the positions shown (FIGURE C-8). Ensure that the serial port jumpers are set correctly.

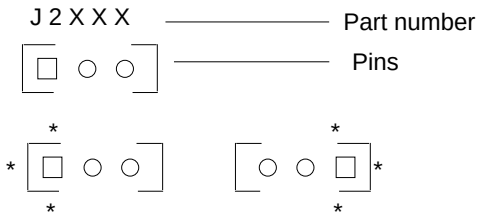

FIGURE C-8 Identifying Jumper Pins

C.5.1 Serial Port Jumpers

Serial port jumpers J2104 and J2105 can be set to either RS-423 or RS-232 serial interface. The jumpers are preset for RS-423. RS-232 is required for digital telecommunication within the European Community. TABLE C-7 identifies serial port jumper settings. If the system is being connected to a public X.25 network, the serial port mode jumper setting may need to change from RS-423 to RS-232 mode.

To change the serial port mode jumper setting:

1. **Power off the system unit.**

   See Section 6.2 “Powering Off the System Unit” on page 6-3.

2. **Remove the system unit cover.**

   See Section 7.1 “Removing the System Unit Cover” on page 7-2.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wriststrap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing it on any surface.

3. **Attach the wrist strap.**

   See Section 7.2 “Attaching the Wrist Strap” on page 7-3.

4. **Locate the jumpers on the motherboard and change the selection of jumpers J2104 and J2105 to position B.**

5. **Detach the wrist strap.**

6. **Replace the system unit cover.**

   See Section 7.3 “Replacing the System Unit Cover” on page 7-4.

7. **Power on the system unit.**

   See Section 6.1 “Powering On the System Unit” on page 6-2.

TABLE C-7 Serial Port Jumper Settings

Jumper	Pins 1 + 2 Select	Pins 2 + 3 Select	Default Jumper on Pins	Signal Controlled
J2104	RS-232	RS-423	2 + 3	RS-232 / RS-423 SEL
J2105	RS-232	RS-423	2 + 3	RS-232 / RS-423 SEL

C.5.2 Flash PROM Jumpers

Flash PROM jumpers J2202, J2203, and J2204 permit the reprogramming of specific code blocks. TABLE C-8 identifies the flash PROM jumper settings. The default setting of J2202 through J2204 is located on pins 1 and 2. TABLE C-8 identifies the signals controlled by the non-default settings of jumpers J2203 and J2004.

TABLE C-8 Flash PROM Jumper Settings

Jumper	Pins 1 + 2 Select	Pins 2 +3 Select	Default Jumper on Pins	Signal Controlled
J2202	Flash PROM	Not to be used	1 + 2	FLASH PROM SEL
J2203	Write Protect	Write Enable	1 + 2	FLASH PROM PROG ENABLE
J2204	High half booting	Normal Booting	2 + 3	XOR LOGIC SET

Note – After reprogramming the system flash PROMs, verify that the flash PROM Write Protect/Enable jumper (J2203) is set to the Write Protect position to ensure system security.

C.5.3 Additional Motherboard Jumper Blocks

Additional motherboard jumper blocks are identified in TABLE C-9 and are listed for information purposes only.

Note – Do not attempt to add jumpers to jumper blocks identified in TABLE C-9.

TABLE C-9 Additional Motherboard Jumper Blocks

Jumper Block ID	Description
J2103	Enable Test Edge Serial Ports Enable (manufacturing only)
J2201	External Reset: jumper pin 1 to pin 2 to force XIR reset; jumper pin 2 to pin 3 to force POR reset
J2202	Manufacturing ROMBO connector

TABLE C-9 Additional Motherboard Jumper Blocks *(Continued)*

Jumper Block ID	Description
J2203	Manufacturing JTAG / Scan test connector
J3402	Enable Test Edge Ethernet Port (manufacturing only)
J3403	Enable Test Edge Ethernet Port (manufacturing only)

C.6 Enclosure

The Sun Ultra 2 series uses an enclosure that reflects style, ergonomics, serviceability, functionality, versatility, and quality. The physical orientation of the enclosure enables you to install it in a rack-mount or desktop position. The enclosure design complies with all necessary environmental and regulatory specifications.

C.6.1 Enclosure Basics

Overall dimensions of the enclosure are 17.86 inches x 17.63 inches x 5.12 inches (45 cm x 45 cm x 13 cm). The enclosure houses:

- One 3.5-inch (88.9-mm) diskette drive
- One 1.6-inch (40.64-mm) CD-ROM drive in an industry standard 1.6-inch bay

Note – The CD-ROM drive slot is used for either the CD-ROM drive or optional 4-mm and 8-mm tape drives.

- Two 1-inch single-connector 3.5-inch hard drives
- Two plug-in UltraSPARC modules
- Sixteen DSIMMs
- Four SBus modules
- One UPA64S graphics module

C.6.2 Enclosure Features

Enclosure features include:

- Good service access for internal upgrades and field replaceable units (FRUs)
- Optimized motherboard layout
- Graphics expansion module (UPA64S connector)
- Processors placed on plug-in modules. Allows for upgrades and conversion from UP to MP system
- Four SBus cards in a 2 x 2 configuration
- All standard connectors and no splitter cables on the rear panel

C.7 Environmental Compliance

The Ultra 2 series meets or exceeds the specifications defined by the “Controlled Office” classification of the 990-1146-03, Rev A document.

C.8 Agency Compliance

The Ultra 2 series complies with international and domestic regulatory requirements for safety, ergonomics, EMI, immunity, electrical, and telecommunication.