

Signal Description

This appendix provides signal descriptions for the Ultra 2 series system unit back panel connectors.

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B.1 Keyboard/Mouse Connector, and Serial Ports A and B Connectors

B.1.1 Keyboard/Mouse Connector

The keyboard/mouse connector is a DIN-8 type connector located on the motherboard back panel. FIGURE B-1 illustrates the keyboard/mouse connector configuration and TABLE B-1 lists the keyboard/mouse connector pin assignments.

Note – All signals are standard TTL levels. The +5 VDC supply is fuse-protected.



FIGURE B-1 Keyboard/Mouse Connector Pin Configuration

TABLE B-1 Keyboard/Mouse Connector Pin Assignments

| Pin | Signal Name | Description |
|------------|--------------------|--------------------|
| 1 | Gnd | Ground |
| 2 | Gnd | Ground |
| 3 | +5 Vdc | +5 Vdc |
| 4 | Mse-rxd | Mouse receive data |
| 5 | Kbd-txd | Keyboard out |
| 6 | Kbd-rxd | Keyboard in |
| 7 | Kbd-pwk | Keyboard power on |
| 8 | +5 Vdc | +5 Vdc |

B.1.2 Serial Port Connector A and B (RS-423/RS-232)

Serial port connectors A and B are DB-25 type connectors located on the motherboard back panel. FIGURE B-2 illustrates the serial port A and serial port B connector configuration and TABLE B-2 lists the serial A and B port connector pin assignments.

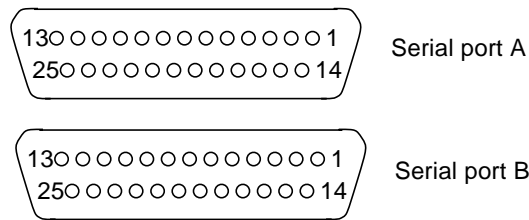


FIGURE B-2 Serial Port A and B Connectors Pin Configuration

TABLE B-2 Serial Port A and B Connectors Pin Assignments

| Pin | Signal Name | I/O | Description |
|-----|---------------|------|---|
| 1 | Not connected | none | None. |
| 2 | TXD | O | Transmit data. Used by the data terminal equipment (DTE) to transmit data to the data circuit equipment (DCE). Except when control data is being sent, RTS, CTS, SYNC, and DCD must be ON for this line to be active. |
| 3 | RXD | I | Receive data. Used by the DCE in response to received data from the DTE. |
| 4 | RTS | O | Ready to send. Used by the DTE to condition the DCE for data transmission. The transition to ON directs the DCE to go into transmit mode. The transition to OFF directs the DCE to complete the transmission. |

TABLE B-2 Serial Port A and B Connectors Pin Assignments (*Continued*)

| Pin | Signal Name | I/O | Description |
|--------|---------------|------|---|
| 5 | CTS | I | Clear to send. Used by the DCE to indicate if it is ready to receive data from the DTE. When CTS, DSR, RTS, and DTR are ON, the DCE is ready to transmit data received from the DTE across the communications channel. When only CTS is ON, the DCE is ready to accept dialing or control signals only. When CTS is OFF, the DTE should not transfer data across TXD. |
| 6 | DSR | I | Data set ready. Used by the DCE to indicate if it is ready to operate. When DSR is ON, the DCE is connected to the line and ready to exchange further control signals to start data transfer. |
| 7 | Gnd | | Signal Ground. |
| 8 | DCD | I | Data carrier detect. Used by the DCE to indicate it is receiving a suitable signal from the communications channel. |
| 9 - 14 | Not connected | none | None. |
| 15 | TRXC | I | Transmit clock. Used by the DCE to provide timing information to the DTE. The DTE provides data on TXD in which the transition of the bit corresponds to the rising edge of the clock. |
| 16 | Not connected | none | None. |
| 17 | RTXC | I | Receive clock. Used by the DCE to provide timing information to the DTE. The falling edge of the clock corresponds to the center of the data bit received on RXD. |
| 18 -19 | Not connected | | None. |
| 20 | DTR | O | Data terminal ready. Used to control switching of the DCE to the communication channel. Once disabled, DTR cannot be enabled until SYNC is turned OFF. |

TABLE B-2 Serial Port A and B Connectors Pin Assignments (*Continued*)

| Pin | Signal Name | I/O | Description |
|------------|--------------------|------------|--|
| 21 - 23 | Not connected | | None. |
| 24 | TXC | O | Terminal clock. Generated by the DTE to provide timing information to the DCE. Used only in Synchronous mode and only when the driver requests a locally generated clock. Otherwise, TXC echoes the modem-generated clock. The falling edge of the clock corresponds to the center of the data bit transmitted on TXD. |
| 25 | Not connected | | None. |

B.2 Twisted-Pair Ethernet Connector

The twisted-pair Ethernet (TPE) connector is an RJ-45 type connector located on the motherboard back panel. FIGURE B-3 illustrates the TPE connector configuration and TABLE B-3 lists the TPE connector pin assignments.



Caution – Connect only TPE cable into TPE connector.



FIGURE B-3 TPE Connector Pin Configuration

TABLE B-3 TPE Connector Pin Assignments

| Pin | Signal Name | Description |
|-----|-------------------------|-----------------|
| 1 | tpe0 | Transmit data + |
| 2 | tpe1 | Transmit data - |
| 3 | tpe2 | Receive data + |
| 4 | Common mode termination | Termination |
| 5 | Common mode termination | Termination |
| 6 | tpe3 | Receive data - |
| 7 | Common mode termination | Termination |
| 8 | Common mode termination | Termination |

B.3 Fast/Wide SCSI Connector

The fast/wide small computer system interface (SCSI) connector is located on the motherboard back panel. FIGURE B-4 illustrates the fast/wide SCSI connector configuration and TABLE B-4 lists the fast/wide SCSI connector pin assignments.

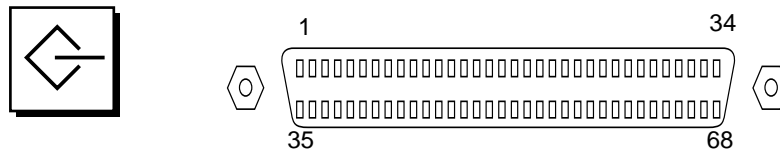


FIGURE B-4 Fast/Wide SCSI Connector Pin Configuration

TABLE B-4 Fast/Wide SCSI Connector Pin Assignments

| Pin | Signal Name | Description |
|---------|-------------|-------------|
| 1 - 16 | Gnd | Ground |
| 17 | Termpower | Termpower |
| 18 | Termpower | Termpower |
| 19 | Not used | Undefined |
| 20 - 34 | Gnd | Ground |
| 35 | Dat<12>_ | Data 12 |
| 36 | Dat<13>_ | Data 13 |
| 37 | Dat<14>_ | Data 14 |
| 38 | Dat<15>_ | Data 15 |
| 39 | Par1 l_ | Parity 1 |
| 40 | Dat<0>_ | Data 0 |
| 41 | Dat<1>_ | Data 1 |
| 42 | Dat<2>_ | Data 2 |

TABLE B-4 Fast/Wide SCSI Connector Pin Assignments (*Continued*)

| Pin | Signal Name | Description |
|------------|--------------------|--------------------|
| 43 | Dat<3>_ | Data 3 |
| 44 | Dat<4>_ | Data 4 |
| 45 | Dat<5>_ | Data 5 |
| 46 | Dat<6>_ | Data 6 |
| 47 | Dat<7>_ | Data 7 |
| 48 | Par0 l_ | Parity 0 |
| 49 | Gnd | Ground |
| 50 | Term_dis_ | Term disable |
| 51 | Termpower | Termpower |
| 52 | Termpower | Termpower |
| 53 | Not used | Undefined |
| 54 | Gnd | Ground |
| 55 | Atn_ | Attention |
| 56 | Gnd | Ground |
| 57 | Bsy_ | Busy |
| 58 | Ack_ | Acknowledge |
| 59 | Rst_ | Reset |
| 60 | Msg_ | Message |
| 61 | Sel_ | Select |
| 62 | Cd_ | Command |
| 63 | Req_ | Request |
| 64 | IO_ | In/Out |
| 65 | Dat<8>_ | Data 8 |

TABLE B-4 Fast/Wide SCSI Connector Pin Assignments (*Continued*)

| Pin | Signal Name | Description |
|------------|--------------------|--------------------|
| 66 | Dat<9>_ | Data 9 |
| 67 | Dat<10>_ | Data 10 |
| 68 | Dat<11>_ | Data 11 |

B.4 Audio Port Connectors

The audio port connectors are located on the motherboard back panel. These ports use EIA standard 0.125-inch (3.5-mm) jacks. FIGURE B-5 illustrates each audio port configuration and TABLE B-5 lists each audio port line assignment.

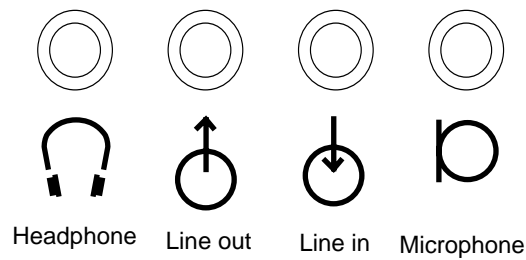


FIGURE B-5 Audio Port Connectors Jack Configuration

TABLE B-5 Audio Port Connectors Line Assignment

| Component | Headphone | Line Out | Line In | Microphone |
|---------------|---------------|---------------|---------------|---------------|
| Tip | Left channel | Left channel | Left channel | Left channel |
| Ring (center) | Right channel | Right channel | Right channel | Right channel |
| Shield | Ground | Ground | Ground | Ground |

B.5 Parallel Port Connector

The parallel port connector is a DB-25 type connector located on the motherboard back panel. FIGURE B-6 illustrates the parallel port connector configuration and TABLE B-6 lists the parallel port connector pin assignments.

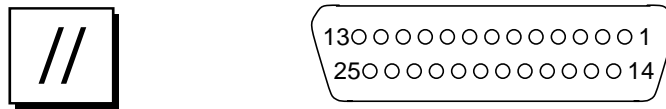


FIGURE B-6 Parallel Port Connector Pin Configuration

TABLE B-6 Parallel Port Connector Pin Assignments

| Pin | Signal Name | Description |
|--------|---------------|---|
| 1 | Data_Strobe_L | Data strobe low. Set low during forward channel transfers to latch data into peripheral device. Set high during reverse channel transfers. |
| 2 to 9 | Data[0..7] | Data0 through Data7. The main data bus for the parallel port. Data0 is the least significant bit (LSB). Pins are not used during reverse channel transfers. |
| 10 | ACK_L | Acknowledge low. Driven low by the peripheral device to acknowledge data byte transfer from host during forward channel transfer. Qualifies data being transferred to host in reverse channel transfer. |
| 11 | BUSY | Busy. Driven high to indicate the peripheral device is not ready to receive data during forward channel transfer. Used to send Data3 and Data7 during reverse channel transfer. |
| 12 | PERROR | Parity error. Driven high by peripheral device to indicate an error in the paper path during forward channel transfer. Used to send Data2 and Data6 during reverse channel transfer. |

TABLE B-6 Parallel Port Connector Pin Assignments (*Continued*)

| Pin | Signal Name | Description |
|---------|---------------|--|
| 13 | SELECT_L | Select low. Indicates the peripheral device is on line during forward channel transfer. Used to send Data1 and Data5 during reverse channel transfer. |
| 14 | AFXN_L | Auto feed low. Set low by the host to drive the peripheral into auto-line feed mode during forward channel transfer. During reverse channel transfer, set low to indicate host can receive peripheral device data and then set high to acknowledge receipt of peripheral data. |
| 15 | ERROR_L | Error low. Set low by the peripheral device to indicate an error during forward channel transfer. In reverse channel transfer, set low to indicate peripheral device has data ready to send to the host. Used to send Data0 and Data4. |
| 16 | INIT_L | Initialize low. Driven low by the host to reset peripheral. |
| 17 | PAR_IN_L | Peripheral input low. Set low by the host to select peripheral device for forward channel transfer. Set high to indicate bus direction is from peripheral to host. |
| 18 - 25 | Signal Ground | Signal ground. |

B.6 Media Independent Interface Connector

The media independent interface (MII) connector (designated J2501) is located on the motherboard back panel. FIGURE B-7 illustrates the MII connector configuration and TABLE B-7 lists the MII connector pin assignment.

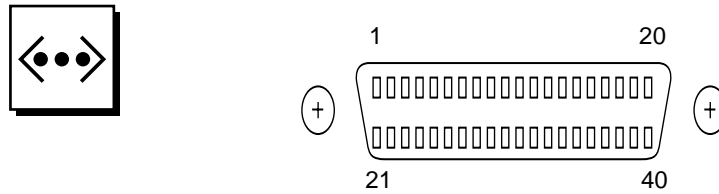


FIGURE B-7 MII Connector Pin Configuration

TABLE B-7 MII Connector Pin Assignments

| Pin | Signal Name | Description |
|-----|-------------|-----------------------|
| 1 | Pwr | Power |
| 2 | Mdio | Management data I/O |
| 3 | Mdc | Management data clock |
| 4 | Rxd3 | Receive data 3 |
| 5 | Rxd2 | Receive data 2 |
| 6 | Rxd1 | Receive data 1 |
| 7 | Rxd0 | Receive data 0 |
| 8 | Rx dv | Receive data valid |
| 9 | Rx clk | Receive clock |
| 10 | Rx er | Receive error |
| 11 | Tx er | Transmit error |
| 12 | Tx clk | Transmit clock |

TABLE B-7 MII Connector Pin Assignments (*Continued*)

| Pin | Signal Name | Description |
|---------|-------------|----------------------|
| 13 | Tx en | Transmit data enable |
| 14 | Txd0 | Transmit data 0 |
| 15 | Txd1 | Transmit data 1 |
| 16 | Txd2 | Transmit data 2 |
| 17 | Txd3 | Transmit data 3 |
| 18 | Col | Collision detected |
| 19 | Crs | Carrier sense |
| 20 | Pwr | Power |
| 21 | Pwr | Power |
| 22 - 39 | Gnd | Ground |
| 40 | Pwr | Power |

B.7 UPA Graphics Card 13W3 Connector

The UPA graphics card 13W3 connector is located on the UPA graphics card. FIGURE B-8 illustrates the UPA graphics card connector configuration and TABLE B-8 lists the UPA graphics card 13W3 connector pin assignments.

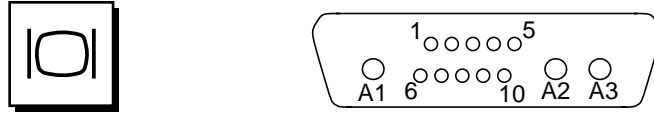


FIGURE B-8 UPA Graphics Card 13W3 Connector Pin Configuration

TABLE B-8 UPA Graphics Card 13W3 Connector Pin Assignments

| Pin | Signal Name | I/O | Description |
|-----|--------------|-----|-----------------|
| A1 | R | O | Red |
| A2 | G | O | Green |
| A3 | B | O | Blue |
| 1 | Serial Read | | Serial Read |
| 2 | Vert Sync | O | Vertical Sync |
| 3 | Sense <0> | I | Sense <0> |
| 4 | Gnd | | Ground |
| 5 | Comp Sync | O | Composite Sync |
| 6 | Horiz Sync | O | Horizontal Sync |
| 7 | Serial Write | | Serial Write |
| 8 | Sense <1> | I | Sense <1> |
| 9 | Sense <2> | I | Sense <2> |
| 10 | Gnd | | Ground |