

Power-On Self-Test

This chapter contains procedures to initiate the power-on self-test (POST) diagnostics. Procedures are also included to support pre-POST preparation, POST data interpretation, and bypassing POST diagnostics. The following is a list of the POST diagnostic topics presented in this chapter.

- POST Overview—page 3-2
- Pre-POST Preparation—page 3-2
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- Maximum and Minimum Levels of POST—page 3-6
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3.1 POST Overview

The POST is useful in determining if a portion of the system has failed and should be replaced. POST detects approximately 85 percent of Ultra 2 series system faults and is located in the system board OpenBoot PROM (OBP). The setting of the diag-level switch determines the POST function. TABLE 3-1 lists the diag-level switch settings for disabling POST (off), enabling POST Maximum (max), or enabling POST Minimum (min).

TABLE 3-1 diag-level switch? and diag-level Flag Settings

diag-level Setting	diag-switch? Setting	POST Initialization	Serial Port A Output
Off	N/A	No	Disabled
N/A	False	No	Disabled
Max	True	Yes (power-on)	Enabled
Min	True	Yes (power-on)	Enabled

3.2 Pre-POST Preparation

Pre-POST preparation includes:

- Setting up a tip connection to another workstation or terminal to view POST progress and error messages. See Section 3.2.1 “Setting Up a Tip Connection” on page 3-3.
- Verifying baud rates between a workstation and a monitor or a workstation and a terminal. See Section 3.2.2 “Verifying the Baud Rate” on page 3-4.

If a terminal or a monitor is not connected to serial port B (default port) of a workstation or server to be tested, the keyboard LEDs are used to determine error conditions. See Section 3.8 “System and Keyboard LEDs” on page 3-17.

3.2.1 Setting Up a Tip Connection

Using a tip connection enables a remote shell window to be used as a terminal to display test data of a system being tested. Serial port A or serial port B of a tested system unit is used to establish the tip connection between the system unit being tested and another Sun workstation monitor or TTY-type terminal. The tip connection is used in a SunOS™ window and provides features to help with the OBP.

To set up a tip connection:

1. See FIGURE 3-1. Connect serial port A of the system being tested to serial port B of another Sun workstation using a serial null modem cable (connect cable pins 2-3, 3-2, 7-20, and 20-7).

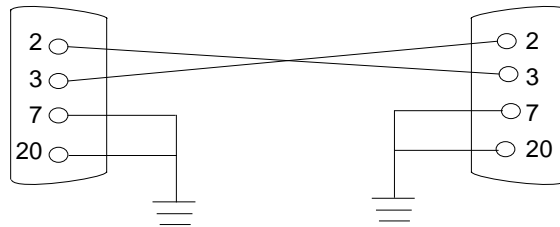


FIGURE 3-1 Setting Up a tip Connection

2. On the other Sun workstation, check the `/etc/remote` file by changing to the `/etc` directory and editing the `remote` file:

```
hardwire:/ dv=/dev/term/b:br#9600:e1=^C^S^Q^U^D:ie=%$:oe=^D:
```

Note – The example shows connection to serial port B.

3. To use serial port A:
 - a. Copy and paste the serial port B `remote` file.
 - b. Modify the serial port B `remote` file by changing the `/b` to `/a`.

```
hardwire:/ dv=/dev/term/b:br#9600:e1=^C^S^Q^U^D:ie=%$:oe=^D:
hardwire:/ dv=/dev/term/a:br#9600:e1=^C^S^Q^U^D:ie=%$:oe=^D:
```

4. In a shell window on the Sun workstation, type `tip hardware`.

```
hostname% tip hardware
connected
```

Note – The shell window is now a tip window directed to the serial port of the system unit being tested. When power is applied to the system unit being tested, POST messages will be displayed in this window.

5. When the POST is completed, disconnect the tip window as follows:

- a. Open a shell window.
- b. Type `ps -a` to view the active tip line and process ID (PID) number.
- c. Type the following to stop the tip hardware process.

```
% kill -9 PID#
```

3.2.2 Verifying the Baud Rate

To verify the baud rate between the system unit being tested and a terminal or another Sun workstation monitor:

1. Open a shell window.
2. Type `eeeprom`.
3. Verify the following serial port default settings as follows:

```
ttyb-mode = 9600,8,n,1
ttya-mode = 9600,8,n,1
```

Note – Ensure that the settings are consistent with TTY-type terminal or workstation monitor settings.

3.3 Initializing POST

POST is initialized in two ways:

- By setting the `diag-switch?` flag to `true` and the `diag-level` flag to `max` or `min`, followed by power cycling the system unit
- By simultaneously pressing the keyboard Stop and D keys while power is applied to the system unit

To set the `diag-switch?` to `true` and power cycle the system unit:

1. At the system prompt, type:

```
ok setenv diag-switch? true
```

2. At the keyboard, power cycle the system unit by simultaneously pressing the Shift key and the Power-on key (FIGURE 3-2). After a few seconds, press the Power-on key again.

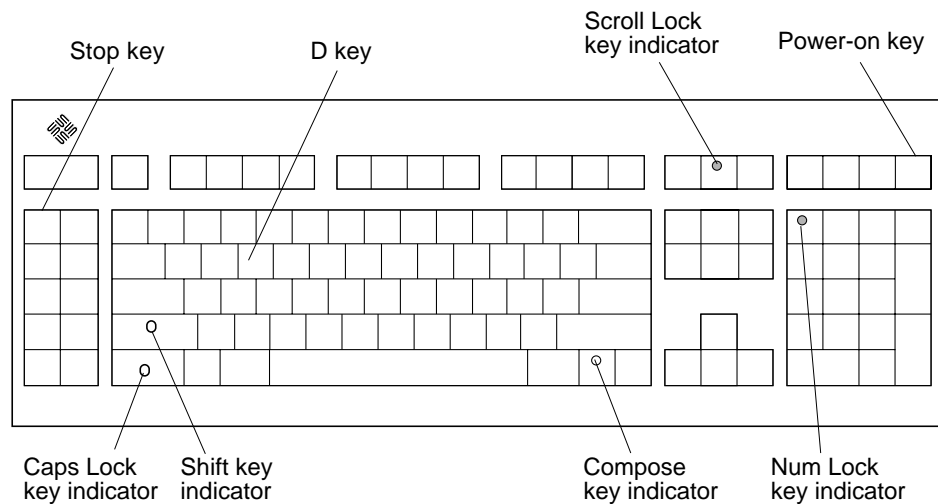


FIGURE 3-2 Sun Type-5 Keyboard

3. Verify the following:

- a. The display prompt is no longer displayed.
- b. The monitor power-on indicator flashes on and off.
- c. The keyboard Caps Lock key indicator flashes on and off.

4. When the POST is complete, type the following at the system prompt:

```
ok setenv diag-switch? false
```

3.4 Maximum and Minimum Levels of POST

Two levels of POST are available: maximum (max) level and minimum (min) level. The system initiates the selected level of POST based upon the setting of `diag-level`, a nonvolatile random access memory (NVRAM) variable.

The default setting for `diag-level` is `max`. An example of a `max` level POST output on serial port A is provided in Section 3.4.1 “Diag-Level NVRAM Variable Set to max” on page 3-7. An example of a `min` level POST output on serial port A is provided in Section 3.4.2 “Diag-Level NVRAM Variable Set to min” on page 3-12.

To set the `diag-level` variable to `min`, type:

```
ok setenv diag-level min
```

To return to the default setting, type the following:

```
ok setenv diag-level max
```

3.4.1 Diag-Level NVRAM Variable Set to max

When the diag-level NVRAM parameter is set to max, POST enables an extended set of diagnostic-level tests. This mode requires approximately 4.5 minutes to complete with a dual CPU configuration and 640 Mbytes of memory installed, or approximately 2.5 minutes to complete with a single CPU configuration and 640 Mbytes of memory installed. CODE EXAMPLE 3-1 identifies a typical serial port A POST output with the diag-level NVRAM variable set to max.

CODE EXAMPLE 3-1 diag-level Variable Set to max

```
{0} ok `Hardware Power ON

Master CPU online
Master Version: 0000.0000.2200.1040
Slave Version: 0000.0000.2200.1040
CPU E$(M) 0000.0000.0010.0000 (S) 0000.0000.0010.0000
Button Power ON

Master CPU online
Master Version: 0000.0000.2200.1040
Slave Version: 0000.0000.2200.1040
CPU E$(M) 0000.0000.0010.0000 (S) 0000.0000.0010.0000
Button Power ON

Master CPU online
Master Version: 0000.0000.2200.1040
Slave Version: 0000.0000.2200.1040
CPU E$(M) 0000.0000.0010.0000 (S) 0000.0000.0010.0000

Probing keyboard Done
%o0 = 0000.0000.0000.4001

Executing Power On SelfTest

0>@(#) Sun Ultra Enterprise 2 FCS_POST, version SB3.3.7 3/09/1998
02:14 PM
1>@(#) Sun Ultra Enterprise 2 FCS_POST, version SB3.3.7 3/09/1998
02:14 PM
0> UltraSparc1 Version 4.0
1> UltraSparc1 Version 4.0
0>Ecache Probe
0> Ecache size 1024 Kb
0>Ecache Tag Test
1>Ecache Probe
1> Ecache size 1024 Kb
1>Ecache Tag Test
```

CODE EXAMPLE 3-1 diag-level Variable Set to max (Continued)

```
0>Ecache RAM Test
1>Ecache RAM Test
0>Ecache Address Line Test
0>Initialize and Verify Ecache
1>Ecache Address Line Test
1>Initialize and Verify Ecache
0>SC Initialization
0>   SC_MP id=acfl, UPA Number=4, Impl=0, Ver=3
0>SC Dual Tag RAM Test
0>   Clearing DTAG's.
0>Initialize SC_MP memory control registers
0>BMX Test
0>   Checking BMX's
0>Probing Memory
0> Found Memory Group #064Mb64Mb64Mb64Mb
0> Found Memory Group #132Mb32Mb32Mb32Mb
0> Found Memory Group #232Mb32Mb32Mb32Mb
0> Found Memory Group #332Mb32Mb32Mb32Mb
0>           Found 640 Megabytes of usable Main Memory
0>SIMM Group      Base Addr      Size      Group Status
0>  0             00000000.00000000    10000000    00
0>  1             00000000.20000000    08000000    00
0>  2             00000000.40000000    08000000    00
0>  3             00000000.60000000    08000000    00
0>Quick Memory Test
0>Clear and Test Stack Memory
0>
    SelfTest Initializing
0>Basic CPU Test
0>   Instruction Cache Tag RAM Test
0>   Instruction Cache Instruction RAM Test
0>   Instruction Cache Next Field RAM Test
0>   Instruction Cache Pre-decode RAM Test
0>   Data Cache RAM Test
0>   Data Cache Tags Test
0>MMU Enable Test
0>   DMMU Registers Access Test
0>   DMMU TLB DATA RAM Access Test
0>   DMMU TLB TAGS Access Test
0>   IMMU Registers Access Test
0>   IMMU TLB DATA RAM Access Test
0>   IMMU TLB TAGS Access Test
0>   DMMU Init
0>   IMMU Init
0>   Mapping Selftest Enabling MMUs
0>FPU Register Test
```

CODE EXAMPLE 3-1 diag-level Variable Set to max (Continued)

```
0> FPU Registers and Data Path Test
0> FSR Read/Write Test
0> EPROMs Test
0> PROM Datapath Test
0> Serial Ports Test
0> Slavio Serial Ports Test
0> NVRAM TOD Test
0> M48T59 (TOD) Init
0> M48T59 (TOD) Functional Part 1 Test
1>
    SelfTest Initializing
1> Basic CPU Test
1> Instruction Cache Tag RAM Test
1> Instruction Cache Instruction RAM Test
1> Instruction Cache Next Field RAM Test
1> Instruction Cache Pre-decode RAM Test
1> Data Cache RAM Test
1> Data Cache Tags Test
1> MMU Enable Test
1> DMMU Registers Access Test
1> DMMU TLB DATA RAM Access Test
1> DMMU TLB TAGS Access Test
1> IMMU Registers Access Test
1> IMMU TLB DATA RAM Access Test
1> IMMU TLB TAGS Access Test
1> DMMU Init
1> IMMU Init
1> Mapping Selftest Enabling MMUs
1> FPU Register Test
1> FPU Registers and Data Path Test
1> FSR Read/Write Test
1> Memory Test
0> Memory Test
1> Memory Clear Test
0> Memory Clear Test
1> Test being relocated into Memory
0> Test being relocated into Memory
1> Memory RAM (blk) Test
0> Memory RAM (blk) Test
1> Test being relocated into Memory
0> Test being relocated into Memory
1> Memory Stress Test
1> Test being relocated into Memory
0> Memory Stress Test
0> Test being relocated into Memory
1> Memory Address Line Test
```

CODE EXAMPLE 3-1 diag-level Variable Set to max (Continued)

```
1> Test being relocated into Memory
0> Memory Address Line Test
0> Test being relocated into Memory
1>CPU Speed
1> CPU 1 Running at 200 MHZ.
0>Forcing ECC Faults Test
0> ECC CE Pattern Test
0> ECC CE Check bit Test
0> ECC UE Pattern Test
0> ECC UE Check bit Test
0>SysIO Registers Test
0> SysIO Register Initialization
0> IOMMU Registers and RAM Test
0> Streaming Buffer Registers and RAM Test
0> SBus Control and Config Registers Test
0> SysIO RAM Initialization
0>SysIO Functional Test
0> Mapping Selftest Enabling MMUs
0> Clear Interrupt Map and State Registers
0> SysIO Interrupts Test
0> SysIO Timers/Counters Test
0> IOMMU Virtual Address TLB Tag Compare Test
0> Streaming Buffer Flush Test
0> DMA Merge Buffer Test
0>CPU Speed
0> CPU 0 Running at 200 MHZ.
0>Ecache Stress Test
0> Ecache Stress Test
0>APC Test
0> APC Registers Tests Test
0> APC DVMA Test
0>Data Cache Test
0> Dcache Init
0> Dcache Enable Test
0> Dcache Functionality Test
0>FEPS Test
0> Parallel Port Registers Test
0> Parallel Port ID is: 0x2
0> Parallel Port DVMA burst mode read/write Test
0> FAS366 Registers Test
0> ESP FAS366 DVMA burst mode read/write Test
0> FEPS Internal Loopbacks Test
0> Ethernet Tranceiver Internal Loopbacks Test
0>CPU Functional Test
1>CPU Functional Test
0> Mapping Selftest Enabling MMUs
```

CODE EXAMPLE 3-1 diag-level Variable Set to max (*Continued*)

```
1> Mapping Selftest Enabling MMUs
0> SPARC Atomic Instructions Test
1> SPARC Atomic Instructions Test
0> CPU Dispatch Control Register Test
1> CPU Dispatch Control Register Test
0> CPU Softint Registers and Interrupts Test
1> CPU Softint Registers and Interrupts Test
0> CPU Tick and Tick Compare Registers Test
1> CPU Tick and Tick Compare Registers Test
0> Uni-Processor Cache Coherence Test
0> Base_address = 00100000
1> Uni-Processor Cache Coherence Test
1> Base_address = 00300000
0> UltraSPARC-2 Prefetch Instructions Test
1> UltraSPARC-2 Prefetch Instructions Test
0> *UltraSparc-1 module detected, tests skipped
1> *UltraSparc-1 module detected, tests skipped
1>..... Processor 1 is in slave-wait phase...
0>Cross Calls Test
0> Cross Calls Test
0>Cache Coherency Test
0> Multi-Processor Cache Coherence Test
0>
    << POST COMPLETE >>
0>**Entering OBP (3b)

Power On Selftest Completed
```

3.4.2 Diag-Level NVRAM Variable Set to min

When the diag-level NVRAM parameter is set to min, POST enables an abbreviated set of diagnostic-level tests. This mode requires approximately 2 minutes to complete with a dual CPU configuration and 640 Mbytes of memory installed, or approximately 45 seconds to complete with a single CPU configuration and 640 Mbytes of memory installed. CODE EXAMPLE 3-2 identifies a serial port A POST output with the diag-level NVRAM variable set to min.

CODE EXAMPLE 3-2 diag-level Variable Set to min

```
Button Power ON

Master CPU online
Master Version: 0000.0000.2200.1040
Slave Version: 0000.0000.2200.1040
CPU E$(M) 0000.0000.0010.0000 (S) 0000.0000.0010.0000
Button Power ON

Master CPU online
Master Version: 0000.0000.2200.1040
Slave Version: 0000.0000.2200.1040
CPU E$(M) 0000.0000.0010.0000 (S) 0000.0000.0010.0000

Probing keyboard Done
%o0 = 0000.0000.0000.2001

Executing Power On SelfTest

0>@(#) Sun Ultra Enterprise 2 FCS_POST, version SB3.3.7 3/09/1998
02:14 PM
1>@(#) Sun Ultra Enterprise 2 FCS_POST, version SB3.3.7 3/09/1998
02:14 PM
0> UltraSparc1 Version 4.0
1> UltraSparc1 Version 4.0
0>
    POST is running with diag-level= min, please wait...
    POST is running with diag-level= min, please wait...
    << POST COMPLETE >>

Power On Selftest Completed
```

3.5 POST Progress and Error Reporting

While POST is initialized, the Caps Lock key on the Sun Type-5 keyboard flashes on and off to indicate that POST tests are being executed. Additional POST progress indications are also visible when a TTY-type terminal or a tip line is connected between serial port B (default port) of the system being tested and a POST monitoring system.

If an error occurs during the POST execution, the keyboard Caps Lock key indicator stops flashing and an error code is displayed using the Caps Lock, Compose, Scroll Lock, and Num Lock key indicators. The error code indicates a particular system hardware failure.

Note – An error code may only be visible for a few seconds. Observe the Caps Lock, Compose, Scroll Lock, and Num Lock key indicators closely while POST is active.

In most cases, POST also attempts to send a failure message to the POST monitoring system. CODE EXAMPLE 3-3 identifies the typical appearance of a failure message. If a keyboard error code is displayed, determine the meaning of the error code by comparing the keyboard error code pattern to the corresponding error code meaning listed in TABLE 3-2.

Note – The system does not automatically boot if a POST error occurs; it halts at the `ok` prompt to alert the user of a failure.

CODE EXAMPLE 3-3 Typical Error Code Failure Message

```
Executing Power On SelfTest

0>@(#) Sun Ultra Enterprise 2 FCS_POST, version SB3.3.7 3/09/1998
02:14 PM
1>@(#) Sun Ultra Enterprise 2 FCS_POST, version SB3.3.7 3/09/1998
02:14 PM
0> UltraSparc1 Version 4.0
1> UltraSparc1 Version 4.0
0>
    POST is running with diag-level= min, please wait...
    POST is running with diag-level= min, please wait...Error:
Mem_group=0 data= 00000000.07070707
0>ERROR: DSIMM's not fully populated/inserted in group_0, POST
terminated
0> Entering OBP(0x00000000)

Power On Selftest Completed
```

TABLE 3-2 Keyboard LED Patterns

Caps Lock	Compose	Scroll Lock	Num Lock	Bit Value	Meaning of Pattern
Blink	Off	Off	Off	x000 ₍₂₎	POST in progress
Off	Off	Off	Off	0000 ₍₂₎	POST successfully completed
Off	Off	Off	On	0001 ₍₂₎	DSIMM in slot U 0401/0501 failed
Off	Off	On	Off	0010 ₍₂₎	DSIMM in slot U 0601/0701 failed
Off	Off	On	On	0011 ₍₂₎	DSIMM in slot U 0402/0502 failed
Off	On	Off	Off	0100 ₍₂₎	DSIMM in slot U 0602/0702 failed
Off	On	Off	On	0101 ₍₂₎	DSIMM in slot U 0403/0503 failed
Off	On	On	Off	0110 ₍₂₎	DSIMM in slot U 0603/0703 failed
Off	On	On	On	0111 ₍₂₎	DSIMM in slot U 0404/0504 failed
On	Off	Off	Off	1000 ₍₂₎	DSIMM in slot U 0604/0704 failed
On	Off	Off	On	1001 ₍₂₎	System board failed
On	Off	On	Off	1010 ₍₂₎	No memory found
On	Off	On	On	1011 ₍₂₎	Reserved
On	On	Off	Off	1100 ₍₂₎	Reserved
On	On	Off	On	1101 ₍₂₎	Reserved
On	On	On	Off	1110 ₍₂₎	Bad CPU0
On	On	On	On	1111 ₍₂₎	Bad CPU1

3.6 Bypassing POST

POST may be disabled and bypassed. To bypass POST:

1. **Prior to powering on the system, press and hold the Stop and D keys on the keyboard (FIGURE 3-2).**
2. **With holding down the keyboard Stop and D keys, press the Power-on to turn on the system unit.**

3.7 Additional Keyboard Control Commands

- Stop Key

If the `diag-level` is set to either `max` or `min` and the `diag-level switch?` variable is set to `true` and POST is not to be executed when the system unit is powered on, press and hold the Stop key and press the Power-on key.

Note – Press and hold the Stop key for approximately 5 seconds.

- Stop and N Keys

To set the system NVRAM parameters to the original default settings, press and hold the Stop and N keys before powering on the system. Continue to hold the Stop and N keys until the system banner is displayed on the monitor.

3.8 System and Keyboard LEDs

The power LED, located at the chassis front, remains lit when the system is operating normally. FIGURE 3-3 shows the location of the power LED.

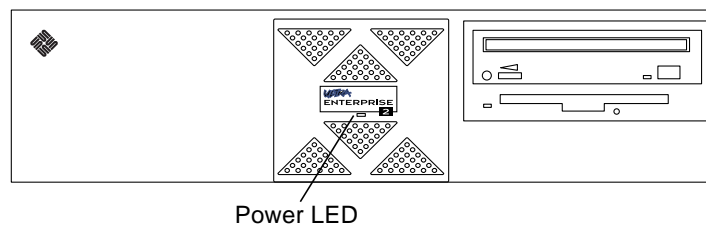


FIGURE 3-3 Power LED

While POST is executing and making progress, the Caps Lock key LED blinks while the rest of the LEDs are off. If POST finds an error, a pattern is encoded in the LEDs to indicate the defective part. If POST completes with no errors, all LEDs will be off and the system will return to the OpenBoot PROM (OBP). TABLE 3-2 on page 3-15 defines the keyboard LED patterns. FIGURE 3-2 shows the location of the LED keys on the keyboard.

3.9 Initializing the Motherboard POST

To initialize the motherboard POST:

1. **Power off the system unit.**
See Section 6.2 “Powering Off the System Unit” on page 6-3.
2. **At the keyboard, simultaneously press and hold the Stop and D keys and press the Power-on key.**

Note – Video output is disabled while POST is initialized.

Note – To view the POST output results, a tip connection must be set up. See Section 3.2.1 “Setting Up a Tip Connection” on page 3-3.

3. **Verify that the keyboard LEDs light to confirm the system is in the POST mode. Verify that the keyboard Caps Lock key LED flashes on and off to indicate the system has enabled POST.**
4. **If a failure occurs during POST, a keyboard key LED other than the Caps Lock key LED may light, indicating a failed system component.**
See Section 3.8 “System and Keyboard LEDs” on page 3-17.
5. **If the Caps Lock key LED fails to flash after the Stop and D keys are pressed, the POST has failed.**
See Section 3.8 “System and Keyboard LEDs” on page 3-17.

Note – The most probable cause of this type of failure is the motherboard. However, optional system components can also cause POST to fail.

6. **Before replacing the motherboard, remove any optional components, such as PCI cards and memory, and repeat the POST.**

Note – Non-optional components such as DSIMMs, the motherboard, the power supply, and the keyboard must be installed for POST to execute properly. Removing the optional system components and retesting the system unit isolates the possibility that those components are the cause of the failure.

7. **To view additional POST failure information, establish a tip connection.**
See Section 3.2.1 “Setting Up a Tip Connection” on page 3-3.